II. Amendments to the Claims:

This listing and version of the claims replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A sensor for electrostatic discharge (ESD) protection, comprising:

an inverter coupled to an output terminal of the sensor;

a voltage drop circuit coupled to an input terminal of the sensor, wherein a voltage drop occurs across the voltage drop circuit and a high state voltage is generated at the output terminal of the sensor when the input terminal of the sensor is coupled to an ESD voltage pulse, thereby applying the high state voltage to the inverter; and

a device coupled to the voltage drop circuit in series, wherein the device is adapted to maintain the high state voltage at the output terminal of the sensor, while the input terminal of the sensor is coupled to the ESD voltage pulse, wherein the device comprises a N-type MOS (NMOS) transistor,

wherein an output of the inverter is coupled to a gate terminal of a MOS transistor of an ESD protection circuit, and

wherein the MOS transistor of the ESD protection circuit is a cascaded NMOS.

2. (Original) The sensor of claim 1, wherein the input terminal of the sensor is coupled to a voltage supply terminal.

3. (Previously Presented) The sensor of claim 1, wherein the voltage drop circuit comprises a series of diodes.

4. (Original) The sensor of claim 3, wherein the series of diodes has about 3 to about 8 diodes.

5-6. (Canceled)

7. (Currently Amended) The sensor of claim [[6]] 1, wherein a gate terminal and a drain terminal of the NMOS transistor are common and coupled to the output terminal of the sensor.

8-11. (Canceled)

12. (Previously Presented) The sensor of claim 1, wherein the gate terminal of the MOS transistor is pulled down to a low state voltage when the input terminal of the sensor is coupled to the ESD voltage pulse.

13. (Currently amended) A circuit for electrostatic discharge (ESD) protection, comprising:

an ESD protection circuit having a stack of cascaded NMOS transistors ~~metal-oxide-semiconductor (MOS) transistor with a gate terminal therein, wherein the MOS transistor is~~ configured to discharge an ESD pulse, ~~wherein the MOS transistor of the ESD protection circuit is a cascaded NMOS comprising at least two NMOS transistors having common gate, source and drain terminals~~;

a sensor that senses the ESD pulse and generates a high state voltage at an output terminal of the sensor in response to the ESD pulse; and

an inverter coupled to the output terminal of the sensor and the ESD circuit, wherein the sensor applies the high state voltage to an input terminal of the inverter.

14. (Currently Amended) The circuit of claim 13, wherein an input to the stack of cascaded NMOS transistors ~~the gate terminal of the MOS transistor~~ of the ESD protection circuit is pulled down to a low state voltage by an output voltage of the inverter when the sensor senses the ESD pulse.

15. (Previously Presented) The circuit of claim 13, wherein the sensor comprises:

a voltage drop circuit coupled to the input terminal of the sensor, wherein a voltage drop occurs across the voltage drop circuit and the high state voltage is generated at the output terminal of the sensor when the input terminal of the sensor is coupled to a voltage generated by the ESD pulse; and

a device coupled to the voltage drop circuit, wherein the device is adapted to maintain the high state voltage at the output terminal, while the input terminal of the sensor is coupled to the ESD voltage pulse.

16. (Original) The circuit of claim 15, wherein the input terminal of the sensor is coupled to a voltage supply terminal.

17. (Previously Presented) The circuit of claim 15, wherein the voltage drop circuit comprises a series of diodes.

18. (Original) The circuit of claim 17, wherein the series of diodes has about 3 to about 8 diodes.

19. (Original) The circuit of claim 15, wherein the device comprises a metal-oxide-semiconductor (MOS) transistor.

20. (Original) The circuit of claim 19, wherein the MOS transistor of the device is a N-type MOS (NMOS) transistor.

21. (Original) The circuit of claim 20, wherein a gate terminal and a drain terminal of the NMOS transistor of the device are common.

22. (Canceled)

23. (Currently Amended) A method for electrostatic discharge (ESD) protection, comprising:

sensing an ESD pulse; and

pulling down an input ~~gate terminal of a MOS transistor~~ of an ESD protection circuit to a low state voltage when the ESD pulse is sensed, wherein the ESD protection circuit comprises stack of cascaded NMOS transistors ~~MOS transistor is~~ configured to discharge the ESD pulse~~, wherein the MOS transistor is a cascaded NMOS comprising at least two NMOS transistors having common gate, source and drain terminals~~.

24. (Original) The method of claim 23, wherein the step of sensing the ESD pulse is performed by a sensor.

25. (Original) The method of claim 24 further comprising connecting the sensor to a voltage supply terminal to sense the ESD pulse.

26. (Original) The method of claim 25 further comprising generating a high state voltage at an output terminal of the sensor when the ESD pulse is sensed.

27. (Original) The method of claim 26 further comprising connecting the output terminal of the sensor to an inverter to generate a low state voltage at an output terminal of the inverter when the ESD pulse is sensed.

28. (Currently Amended) The method of claim 27 further comprising connecting the output terminal of the inverter to the input of ~~the gate terminal of the MOS transistor of~~ the ESD protection circuit.